

10D05

July 18, 2001

Re: 09/781,120 (US 5,870,296)

Dear Examiner Berhane,

Attached are the requested litigation search results.

Several patent litigation and news databases were searched using Dialog, Lexis-Nexis and Questel-Orbit search systems.

No litigation cases were found to be associated with this patent number.

Thank you for using EIC2800!

Paul Schulwitz
308-6559
CP4-9C18

Source: [All Sources](#) > [Area of Law - By Topic](#) > [Patent Law](#) > [Patents](#) > [U.S. Patents](#) > [Utility Patents](#) (f)Terms: **patno is 5,870,296** ([Edit Search](#))*Pat. No. 5870296, ****5,870,296**◆ GET 1st DRAWING SHEET OF 4

Feb. 9, 1999

Dual interleaved DC to DC switching circuits realized in an integrated circuit

REISSUE: Reissue Application filed Jan. 8, 2001 (O.G. Apr. 17, 2001) Ex. Gp.: 2838; Re. S.N. 09/781,120**INVENTOR:** Schaffer, Gregory L., Cupertino, California**ASSIGNEE-AT-ISSUE:** Maxim Integrated Products, Inc., Sunnyvale, California (02)**APPL-NO:** 949,463**FILED:** Oct. 14, 1997**INT-CL:** [6] H02M 7#00**US-CL:** 363#65; 323#282**CL:** 363;323**SEARCH-FLD:** 323#282; 363#65, 26**REF-CITED:****U.S. PATENT DOCUMENTS**

4,489,370	12/1984	* Migliori	363#26
5,583,753	12/1996	* Takayama	363#65
5,604,669	2/1997	* Strong, III	363#26
5,719,491	2/1998	* Kolanko et al.	323#282
5,764,007	6/1998	* Jones	318#109
5,781,421	7/1998	* Steigerwald et al.	363#65

PRIM-EXMR: Hecker, Stuart N.**LEGAL-REP:** Blakely, Sokoloff, Taylor & Zafman LLP**CORE TERMS:** voltage, input, transistor, converter, gate, resistor, load, output voltage, amplifier, interleaved, pulse, capacitor, inverter, modulator, width, comparator, switching circuit, integrated, responsive, inductor, switching, cycle, external, p-channel, differentiator, n-channel, feedback, proportional, driving, dual**ABST:**

Dual interleaved DC to DC switching circuits realizable in an integrated circuit form, capable of monitoring individual inductor current using only one current sense resistor and providing

1/1 PLUSPAT - (C) QUESTEL-ORBIT

PN - US5870296 A 19990209 [US5870296]

TI - (A) Dual interleaved DC to DC switching circuits realized in an integrated circuit

PA - (A) MAXIM INTEGRATED PRODUCTS (US)

IN - (A) SCHAFFER GREGORY L (US)

AP - US94946397 19971014 [1997US-0949463]

PR - US94946397 19971014 [1997US-0949463]

IC - (A) H02M-007/00

EC - H02M-003/158P

PCL - ORIGINAL (O) : 363065000; CROSS-REFERENCE (X) : 323282000

DT - Basic

CT - US4489370; US5583753; US5604669; US5719491; US5764007; US5781421

STG - (A) United States patent

AB - Dual interleaved DC to DC switching circuits realizable in an integrated circuit form, capable of monitoring individual inductor current using only one current sense resistor and providing automatic duty cycle adjustment to keep the inductor currents in the interleaved DC to DC switching circuits balanced. The preferred embodiment includes a gain error amplifier, an integral error amplifier, and a differentiator error amplifier and circuits for controlling the nominal duty cycle, with the gain error amplifier, integral error amplifier and differentiator error amplifier being adjustable independently by external components. The circuit further includes a high speed load regulation circuit that momentarily overrides the control circuitry to take over control of the interleaved converters during sudden load changes, such control also being programmable. The circuit further includes a load variation circuit to target the output voltage of the circuit to an optimal value with load to better keep the output voltage within a targeted range in the event of major step changes in the load. The disclosed embodiment is for two interleaved buck converters, though the principles of the invention are applicable to interleaved step up converters and the interleaving of more than two converters.

1/1 LGST - (C) LEGSTAT

PN - US 5870296 [US5870296]

AP - US 949463/97 19971014 [1997US-0949463]

DT - US-P

ACT - 19971014 US/AE-A

APPLICATION DATA (PATENT)

{US 949463/97 19971014 [1997US-0949463]}

- 19971014 US/AS02

ASSIGNMENT OF ASSIGNOR'S INTEREST

MAXIM INTEGRATED PRODUCTS, INC. 120 SAN GABRIEL DRIVE SUNNYVALE,
CALIFORNIA 9408 * SCHAFFER, GREGORY L. : 19971013

- 19990209 US/A

PATENT

- 20010417 US/RF

REISSUE APPLICATION FILED

20010108

UP - 2001-19

1/1 CRXX - (C) CLAIMS/RRX

AN - 3109840

PN - 5,870,296 A 19990209 [US5870296]

PA - Maxim Integrated Products

PT - E (Electrical)
ACT - 20010108 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20010417
REISSUE REQUEST NUMBER: 09/781120
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2838

Reissue Patent Number:

UP - 2001-16
UACT- 2001-04-17

1/1 PAST - (C) PAST
AN - 200116-002089
PN - 5870296 A [US5870296]
DT - A (UTILITY)
OG - 2001-04-17
CO - REA
ACT - REISSUE APPLICATION FILED
SH - REISSUE APPLICATION FILED

1/39/1

DIALOG(R) File 345:Inpadoc/Fam.& Legal Stat
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14952421

Basic Patent (No,Kind,Date): US 5870296 A 19990209 <No. of Patents: 003>

Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date
EP 1023767	A1	20000802	EP 98949802	A	19981008
US 5870296	A	19990209	US 949463	A	19971014 (BASIC)
WO 9919975	A1	19990422	WO 98US21348	A	19981008

Priority Data (No,Kind,Date):

WO 98US21348 W 19981008

US 949463 A 19971014

PATENT FAMILY:

EUROPEAN PATENT OFFICE (EP)

Patent (No,Kind,Date): EP 1023767 A1 20000802

IC FOR CONTROLLING DUAL INTERLEAVED DC/DC CONVERTERS (English; French;
German)

Patent Assignee: MAXIM INTEGRATED PRODUCTS (US)

Author (Inventor): SCHAFFER GREGORY L (US)

Priority (No,Kind,Date): WO 98US21348 W 19981008; US 949463 A
19971014

Applic (No,Kind,Date): EP 98949802 A 19981008

Designated States: (National) DE; GB; IE; IT; NL

IPC: * H02M-003/158

Derwent WPI Acc No: * G 99-153094

Language of Document: English

EUROPEAN PATENT OFFICE (EP)

Legal Status (No,Type,Date,Code,Text):

EP 1023767 P 19971014 EP AA PRIORITY (PATENT
APPLICATION) (PRIORITAET (PATENTANMELDUNG))

EP 1023767 P 19981008 EP AA PCT-APPLICATION
(PCT-ANMELDUNG)

EP 1023767 P 19981008 EP AE EP-APPLICATION
(EUROPAEISCHE ANMELDUNG)

EP 1023767 P 20000802 EP AK DESIGNATED CONTRACTING
STATES IN AN APPLICATION WITH SEARCH REPORT:
(IN EINER ANMELDUNG BENANNT VERTRAGSSTAATEN)

EP 1023767 P 20000802 EP A1 PUBLICATION OF APPLICATION
WITH SEARCH REPORT (VEROEFFENTLICHUNG DER
ANMELDUNG MIT RECHERCHENBERICHT)

EP 1023767 P 20000802 EP 17P REQUEST FOR EXAMINATION
FILED (PRUEFUNGSANTRAG GESTELLT)
20000428

UNITED STATES OF AMERICA (US)

Patent (No,Kind,Date): US 5870296 A 19990209

DUAL INTERLEAVED DC TO DC SWITCHING CIRCUITS REALIZED IN AN INTEGRATED

CIRCUIT (English)

Patent Assignee: MAXIM INTEGRATED PRODUCTS (US)
Author (Inventor): SCHAFFER GREGORY L (US)
Priority (No,Kind,Date): US 949463 A 19971014
Applic (No,Kind,Date): US 949463 A 19971014
National Class: * 363065000; 323282000
IPC: * H02M-007/00
Derwent WPI Acc No: * G 99-153094; G 99-153094
Language of Document: English

UNITED STATES OF AMERICA (US)

Legal Status (No,Type,Date,Code,Text):

US 5870296 P 19971014 US AE APPLICATION DATA (PATENT)
(APPL. DATA (PATENT))
US 949463 A 19971014
US 5870296 P 19971014 US AS02 ASSIGNMENT OF ASSIGNOR'S
INTEREST
MAXIM INTEGRATED PRODUCTS, INC. 120 SAN
GABRIEL DRIVE SUNNYVALE, CALIFORNIA 9408 ;
SCHAFFER, GREGORY L. : 19971013
US 5870296 P 19990209 US A PATENT
US 5870296 P 20010417 US RF REISSUE APPLICATION FILED
(REISSUE APPL. FILED)
20010108

WORLD INTELLECTUAL PROPERTY ORGANIZATION, PCT (WO)

Patent (No,Kind,Date): WO 9919975 A1 19990422

IC FOR CONTROLLING DUAL INTERLEAVED DC/DC CONVERTERS (English)

Patent Assignee: MAXIM INTEGRATED PRODUCTS (US)

Author (Inventor): SCHAFFER GREGORY L

Priority (No,Kind,Date): US 949463 A 19971014

Applic (No,Kind,Date): WO 98US21348 A 19981008

Designated States: (National) JP; SG (Regional) AT; BE; CH; CY; DE;
DK; ES; FI; FR; GB; GR; IE; IT; LU; MC; NL; PT; SE

Filing Details: WO 100000 With international search report

IPC: * H02M-003/158

Derwent WPI Acc No: * G 99-153094

Language of Document: English

WORLD INTELLECTUAL PROPERTY ORGANIZATION, PCT (WO)

Legal Status (No,Type,Date,Code,Text):


WO 9919975 P 19971014 WO AA PRIORITY (PATENT)
US 949463 A 19971014
WO 9919975 P 19981008 WO AE APPLICATION DATA (APPL.
DATA)
WO 98US21348 A 19981008
WO 9919975 P 19990422 WO AK DESIGNATED STATES CITED IN A
PUBLISHED APPLICATION WITH SEARCH REPORT
(DESIGNATED STATES CITED IN A PUBLISHED APPL.
WITH SEARCH REPORT)
JP SG
WO 9919975 P 19990422 WO AL DESIGNATED COUNTRIES FOR
REGIONAL PATENTS CITED IN A PUBLISHED
APPLICATION WITH SEARCH REPORT (DESIGNATED
COUNTRIES FOR REGIONAL PATENTS CITED IN A
PUBLISHED APPL. WITH SEARCH REPORT)
AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC
NL PT SE

WO 9919975 P 19990422 WO A1 PUBLICATION OF THE
INTERNATIONAL APPLICATION WITH THE
INTERNATIONAL SEARCH REPORT (PUB. OF THE
INTERNATIONAL APPL. WITH THE INTERNATIONAL
SEARCH REPORT)

WO 9919975 P 19990630 WO 121 EP: PCT APP. ART. 158 (1)
(EP: PCT ANM. ART. 158 (1))

WO 9919975 P 19990805 WO DFPE REQUEST FOR PRELIMINARY
EXAMINATION FILED PRIOR TO EXPIRATION OF 19TH
MONTH FROM PRIORITY DATE

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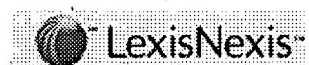
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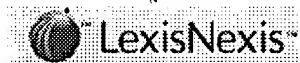
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